RC7100

100MHz Motherboard System Clock

Features

- Four copies of CPU clock
- Eight copies of PCI Clock (Synchronous w/CPU clock)
- Two copies of IOAPIC clock @ 14.318MHz
- Two copies of 48MHz clock
- Three copies of REF clock @ 14.318MHz
- Reference crystal oscillator (14.318MHz)
- Spread Spectrum (-0.5%) clocking
- Power management controls
- Low frequency test mode

Applications

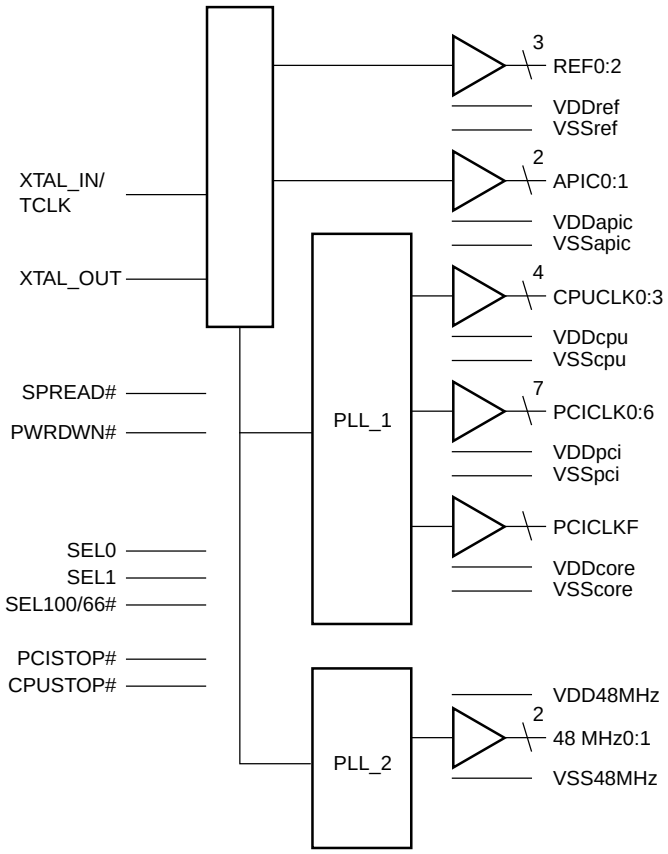
- 100MHz motherboard clock synthesizers for Pentium II CPU based Desktop and Notebook Systems.

Description

The RC7100 is a clock synthesizer for 100MHz operation on Pentium II based motherboard systems.
It contains 4 copies of the CPU clock, 8 copies of the PCI clock, 3 copies of the REF clock, 2 copies of the 48MHz clock and 2 copies of the IOAPIC clock. The CPU and PCI clocks are generated through a phase locked loop and are stable within 3mS after power-up meeting the Pentium II stabilization specifications. The 48MHz clocks are generated through a second phase locked loop.

The RC7100 accepts a 14.318MHz crystal as its reference frequency and operates at a core voltage of 3.3V. A 14.318MHz external clock can also be used instead of the

Block Diagram



Advanced Information

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Description (continued)

crystal. The REF and IOAPIC clocks are generated directly from the reference frequency.

The PWRDWN# pin when low powers down the crystal oscillator and the two phase locked loops. Other pins to control power are the CPUSTOP# and PCISTOP#. The CPUSTOP# when low causes the CPU clocks to go to a low state. The PCISTOP# when low causes the PCI clocks with the exception of the PCICLK_F to go to a low state. The PCICLK_F is a free-running clock. All clock outputs will be tristated when SEL0, SEL1 and SEL100/66# are all low.

Frequency selection between 100 MHz and 66 MHz can be accomplished with the SEL100/66#. SEL100/66# high will provide the 100 MHz operation and low will provide a clock frequency of 66 MHz. Additional frequency selections including TEST MODE can be had with other combinations of the SEL0 and SEL1 pins. See Table 1 for more details.

Spread Spectrum clocking is available for the CPU and PCI clocks. It can be activated by bringing the SPREAD# pin to a low state. the REF, IOAPIC and 48MHz clocks are not affected by the SPREAD#.

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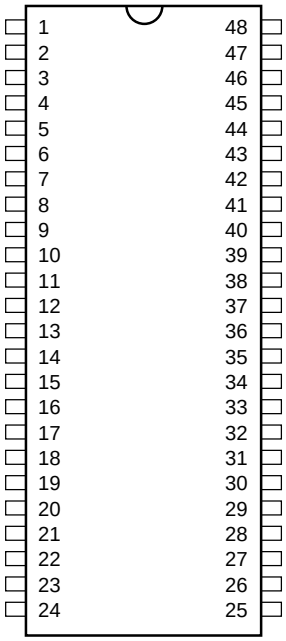
Table 1. Selectable Modes

SEL0	SEL 1	SEL100/66	CPU	PCI	REF	IOAPIC	48
0	0	0	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
1	0	0	75	37.5	14.318	14.318	48
0	1	0	75	30	14.318	14.318	48
1	1	0	66	33	14.318	14.318	48
0	0	1	TC/2	TC/6	TC/2	TC	TC
1	0	1	83.3	41.65	14.318	14.318	48
0	1	1	83.3	33.3	14.318	14.318	48
1	1	1	100	33	14.318	14.318	48

Pin Assignments



Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	REF0	13	PCICLK3	25	SEL100/66#	37	VDDcpu
2	REF1	14	PCICLK4	26	SEL1	38	VSScpu
3	VSSref	15	VDDpci	27	SEL0	39	CPUCLK1
4	XTALIN	16	PCICLK5	28	SPREAD#	40	CPUCLK0
5	XTALOUT	17	PCICLK6	29	PWRDWN#	41	VDDcpu
6	VSSpci	18	VSSpci	30	CPUSTOP#	42	NC
7	PCICLKF	19	VDDcore	31	PCISTOP#	43	VSSapic
8	PCICLK0	20	VSScore	32	VSScore	44	APIC1
9	VDDpci	21	VDD48MHz	33	VDDcore	45	APIC0
10	PCICLK1	22	48MHz0	34	VSScpu	46	VDDapic
11	PCICLK2	23	48MHz1	35	CPUCLK3	47	REF2
12	VSSpci	24	VSS48MHz	36	CPUCLK2	48	VDDref

Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
REF0:2	2, 1, 47	OUT	Reference clock outputs running at a fixed frequency equal to the reference crystal or external frequency (14.318MHz). These operate from a 3.3V power source.
APIC0:1	44, 45	OUT	APIC clocks running at a fixed frequency equal to the reference crystal or external frequency. It is usually 14.318MHz. These operate from a 2.5V power source.
CPUCLK0:3	35, 36, 39, 40	OUT	CPU clocks used to drive the CPU processor. These clock outputs operate from a 2.5V power source.
PCICLKF	7	OUT	Free-running PCI clock which is not affected by PCISTOP#.
PCICLK0:6	8, 10, 11, 13, 14, 16, 17	OUT	PCI clocks for generating all PCI timing requirements. These clock outputs operate from a 3.3V power source.
48MHz0:1	22, 23	OUT	48MHz clocks are fixed frequency outputs for USB or super I/O requirements.
XTALIN	4	IN	Crystal oscillator input or external reference generator input.
XTALOUT	5	OUT	Crystal oscillator output.
SEL100/66#	25	IN	Selects 100MHz or 66MHz for CPU clocks. When this input is at a “1” level, the CPU frequency will be 100MHz and if at a “0” level the frequency will be 66MHz.
SEL1, SEL0	26, 27	IN	Control select pins for selecting different modes of operation.
PWRDWN#	29	IN	PWRDWN# is an input pin used to power-down the chip when low.
PCISTOP#	31	IN	Stops PCI clocks at low state when low
CPUSTOP#	30	IN	Stops CPU clocks at a low state when low
SPREAD#	28	IN	SPREAD# is active low and when activated the CPU and PCI clocks are spread from 0.5% below the maximum frequency to the maximum frequency.
VDDpci, VDDref, VDDcore, VDD48MHz	9, 15, 19, 21, 33, 48	POWER	3.3V supply for PCICLK, PCICLKF, REF, 48MHz drivers and PLL core
VDDcpu, VDDapic	37, 41, 46	POWER	2.5V supply for CPU and APIC drivers
VSSref, VSSpci, VSS48MHz, VSScore, VSScpu, VSSapic	3, 6, 12, 18, 20, 24, 32, 34, 38, 43	GROUND	Ground
NC	42	reserved	No connect - reserved for future use

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Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, VDD	-0.5		5	V
Input Voltage	-0.5		V_{DD}+.5	V
Output, Applied Voltage	-0.5		V_{DD}+.5	V
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering (10 seconds)			300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter	Min.	Typ.	Max.	Units
VDDapic 2.5V Power Supply Voltage VDDcpu	2.375	2.5	2.625	V
VDDref 3.3V Power Supply Voltage VDD48MHz VDDpci VDDcore	3.135	3.3	3.465	V
Ambient Temperature	0		70	°C

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Electrical Characteristics

Parameter		Min.	Typ.	Max.	Units
Logic inputs					
V_{IL}	Input low voltage	-0.3		0.8	V
V_{IH}	Input high voltage	2.0		VDD+.3	V
I_{IL}	Input low current			-5	μA
I_{IH}	Input high current			5	μA
Clock Outputs					
V_{OL}	Outputs @ 1mA			0.4	V
V_{OH}	Outputs @ -1mA	2.4			V
I_{OL}	CPU0:3@ vol = 1.4V	28		100	mA
	PCI_F, PCI1:7 @ vol = 1.4V	26.5		139	mA
	APIC0:1 @ vol = 1.4V	42		150	mA
	REF0:2 @ vol = 1.4V	25		76	mA
	48MHz0:1 @ vol = 1.4V	25		76	mA
I_{OH}	CPU0:3 @ voh = 1.4V	-24		-94	mA
	PCI_F, PCI1:7 @ voh = 1.4V	-31		-189	mA
	APIC0:1 @ voh = 1.4V	-36		-140	mA
	REF0:2 @ voh = 1.4V	-27		-94	mA
	48MHz0:1 @ voh = 1.4V	-27		-94	mA
Crystal oscillator					
V_{TH}	Input threshold voltage				V
C_{LOAD}	Load capacitance imposed on external crystal		18		pF
C_{IN}(XIN)	Input capacitance	13.5	18	22.5	pF
Pin Capacitance/Inductance					
C_{IN}	Input Pin Capacitance			5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Input Pin Inductance			7	nH

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Switching Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
CPU Clocks CPU0:3	C_{LOAD} = 20pF				
Period	100MHz 66MHz	10 15		10.5 15.5	nS
High time	100MHz 66MHz	3.0 5.2			nS
Low time	100MHz 66MHz	2.8 5.0			nS
Tr	100MHz, 66MHz	0.4		1.6	nS
Tf	100MHz, 66MHz	0.4		1.6	nS
tjitter	100MHz, 66MHz			250	pS
Duty cycle @ V = 1.25V	100MHz, 66MHz	45		55	%
tskew	100MHz, 66MHz			175	pS
tpZL, tpZH	100MHz, 66MHz	1.0		8.0	nS
tpLZ, tpHZ	100MHz, 66MHz	1.0		8.0	nS
tstabilization	100MHz, 66MHz			3.0	mS
toffset (CPU to PCI)	100MHz, 66MHz	1.5		4.0	nS
IOAPIC APIC0:1					
tskew	100MHz, 66MHz			250	pS
PCI PCICLK_F, PCICLK1:7					
tperiod	100MHz, 66MHz	30.0			nS
tperiod stability	100MHz, 66MHz			500	pS
thigh	100MHz, 66MHz	12.0			nS
tlow	100MHz, 66MHz	12.0			nS
tskew	100MHz, 66MHz			500	pS
tstabilization	100MHz, 66MHz			3	mS

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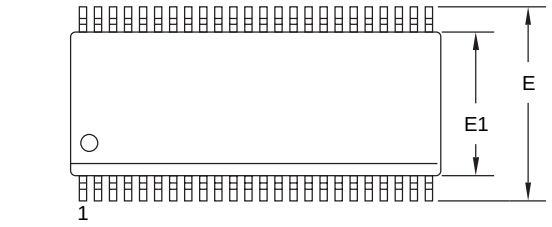
Mechanical Dimensions

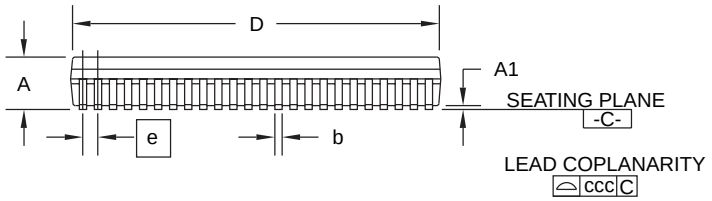
48 pin SSOP

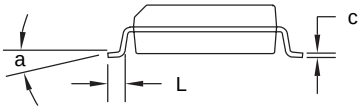
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







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Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7100	0°C to 70°C		48 SSOP	RC7100

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